FSO20N9P7G1

N-Channel *e*MOS Power Trench MOSFET

200 V, 130 A, 9.7 mΩ

Features

- Reduced switching and conduction losses
- Enhanced body diode dV/dt and dI/dt capability
- Robust avalanche capability
- 100% avalanche tested
- Pb-free, Halogen free, and RoHS compliant

Benefits

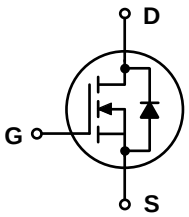
- High system reliability
- System efficiency improvement
- Higher frequency applicability
- Increased power density

Applications

- Motor control
- EV DC-DC & traction inverter
- Battery protection & power tool
- Synchronous rectification
- Micro solar Inverter & UPS

$BV_{DSS,\ Tc=25℃}$	$I_{D,\ Tc=25℃}$	$R_{DS(on),\ max}$	$Q_{g,\ typ}$
200 V	130 A	9.7 mΩ	223 nC

Die Configuration



*Drain: Bottom

Electrical Characteristics (T_J = 25℃, Note1)

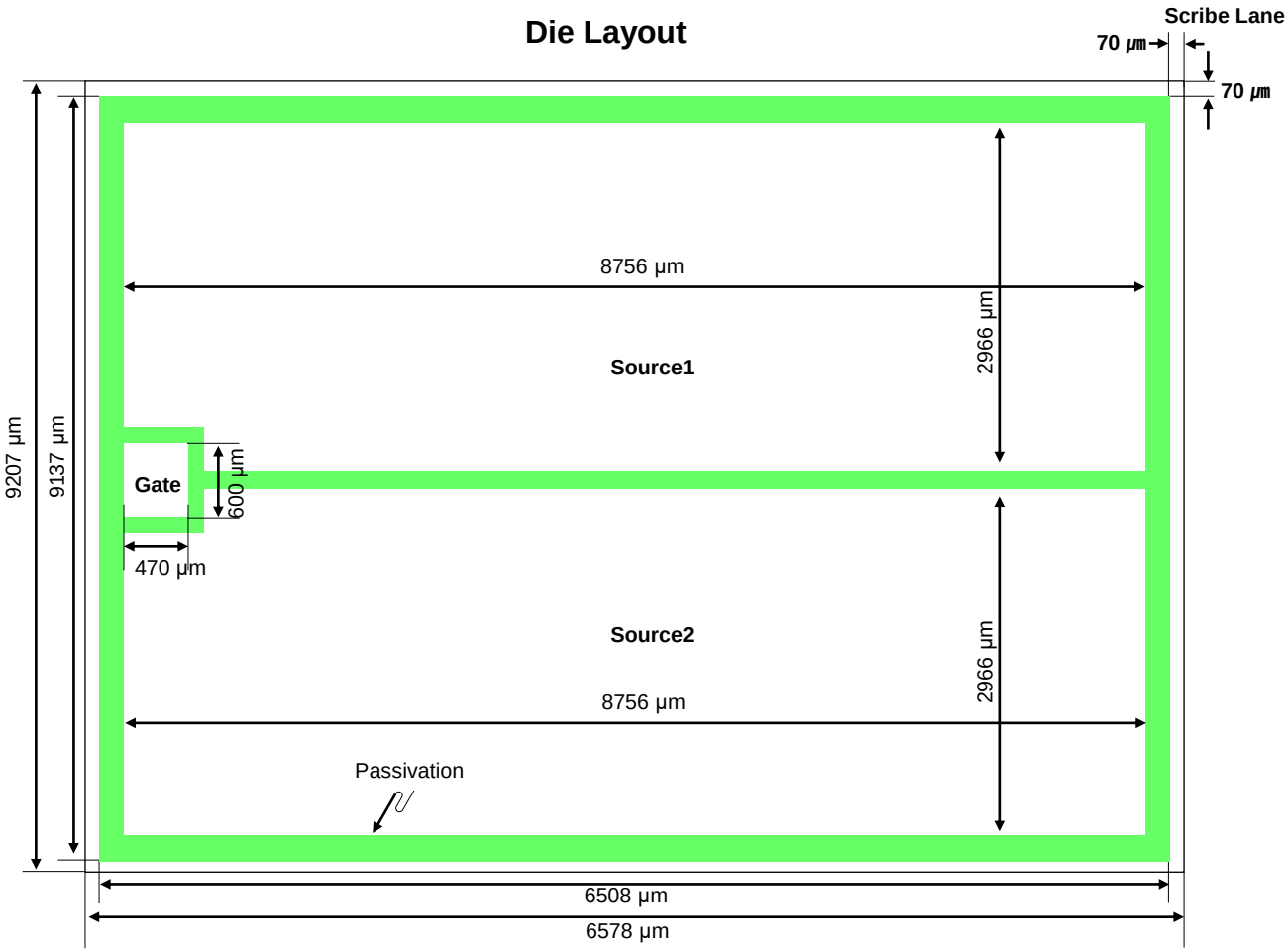
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	200			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 200 V, V_{GS} = 0 V			20	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0		5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 81 A			9.7	mΩ
V_{SD}	Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 81 A			1.3	V

Die Mechanical Parameters

Parameter	Typical Value	Unit
Wafer Diameter	8	inch
Die Dimensions (W x L x T)	9137 x 6508 x 260	μm
Top Side Gate & Source Metallization (AlCu)	5	μm
Bottom Drain Metallization (Ti/Ni/Ag)	1.5	μm
Gate Pad Dimensions (W x L)	470 x 600	μm
Recommended Gate Bond Wire	Al 5mils x 1	ea
Recommended Source Bond Wire	Al 20mils x 3	ea
Gross Die (Single chip of wafer)	430	ea

※Note 1 : 100% tested on wafer.

Die Layout



Wafer Sawing Information